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Description

[METHOD FOR FORMING AN OXIDE/ NITRIDE/OXIDE STACKED LAYER]

BACKGROUND OF INVENTION

[0001] Field of Invention

[0002] The present invention relates to a fabrication method for an oxide/nitride/ oxide (ONO) stacked layer. More particularly, the present invention relates to a fabrication method for a silicon oxide/silicon nitride/silicon oxide stacked layer where damage induced upon the silicon nitride layer due to electron injection and ejection is mitigated.

[0003] Description of Related Art

[0004] A typical flash memory device comprises a polysilicon gate and an oxide/nitride/oxide (ONO) stacked layer structure. The ONO stacked layer includes a bottom silicon oxide layer overlying the channel region. A silicon nitride layer serving as an electron trapping layer overlies

the bottom silicon oxide layer and an upper silicon oxide layer overlies the silicon nitride layer. An ion implantation process is further performed on the substrate to form a source/drain region in the substrate adjacent to the two ends of the silicon nitride layer.

[0005] During the programming of the memory device, electrical charges are transferred from the substrate to the silicon nitride layer in the ONO stacked layer. Voltages are applied to the gate and the drain creating vertical and lateral electric fields which accelerate the electrons along the channel. As the electrons move along the channel, some electrons would gain sufficient energy to jump over the potential barrier of the bottom oxide layer to become trapped in the silicon nitride layer. Electrons are trapped near the drain region because the electric fields are the strongest near the drain. Reversing the potentials applied to the source and the drain will cause electrons to travel along the channel in the opposite direction and be injected into the silicon nitride layer near the source region.

[0006] However, subsequent to multiple times of the electron injection and ejection operation performed on the silicon nitride layer, damages may induce upon the silicon nitride layer. Consequently, current leakage may occur to ad-

versely affect the reliability of the memory device.

SUMMARY OF INVENTION

[0007] The present invention provides a fabrication method for an ONO structure layer, wherein a sturdy interface layer is formed between the silicon nitride layer and the bottom oxide layer to mitigate damages induced upon the silicon nitride layer due to electron injection and ejection.

[0008] The present invention further provides a fabrication method for a silicon nitride layer, wherein variation of the breakdown voltage of the memory device formed with the silicon nitride layer according to the present invention is smaller.

[0009] The present invention provides a fabrication method for a silicon oxide/silicon nitride/silicon oxide stacked layer. A silicon oxide layer is formed over a substrate surface. A surface treatment process is then performed on the first silicon oxide layer. The surface treatment process comprises an in-situ treatment with nitrogen gas. Subsequent to the surface treatment, an interface layer, which serves as a nucleation layer for the subsequently deposited silicon nitride layer, is formed over the silicon oxide layer.

[0010] In accordance to the present invention, a sturdy interface layer is formed between the bottom oxide layer 102 and

the silicon nitride layer 106. The integrity of the silicon nitride layer 106 is maintained even after multiple times of the electron injection and ejection operation.

[0011] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0013] Figure 1A to 1C are schematic cross-sectional views, showing the manufacturing of a silicon oxide/silicon nitride/silicon oxide stacked layer structure according to one aspect of the present invention.

Detailed Description

[0014] Referring to Figure 1A, a substrate 100 is provided. The substrate 100 is, for example, a silicon substrate, which may include numerous devices formed thereon and

therein. An oxide layer 102 is then formed on the substrate 100. The oxide layer 102 is formed by thermal oxidation or by deposition.

[0015] Referring to Figure 1B, subsequent to the formation of the oxide layer 102, an in-situ treatment process is performed on the oxide layer 102. The treatment process comprises a surface treatment process performed in a nitrogen ambient on the oxide layer 102. The treatment process is conducted, for example, with ammonium (NH_3), under a pressure of about 10 torr to 80 torr, at a temperature of about 650 degrees Celsius to 800 degrees Celsius, preferably around 800 degrees Celsius for about 1 to 2 hours.

[0016] In another aspect of the present invention, the treatment process is accomplished through rapid thermal processing. The rapid thermal process is conducted at a temperature of about 650 degrees Celsius to about 1100 degrees Celsius for about 30 to 90 seconds. Subsequent to the surface treatment process, an interface layer 104 is formed on the surface of the oxide layer 102. The interface layer 104 is, for example, a silicon oxynitride (SiO_xN_y) layer. The interface layer 104 is about 20 angstroms thick.

[0017] Continuing to Figure 1C, using the interface layer 104 as a

seed layer, a silicon nitride layer 106 is formed. Thereafter, an oxide layer 108 is formed over the silicon nitride layer 106.

[0018] In accordance to the present invention, an interface layer 104 is formed between the silicon oxide layer 102 and the silicon nitride layer 106. Therefore, the quality and the integrity of the silicon nitride layer 106 are maintained even after multiple times of the electron injection and ejection.

[0019] Further, since the quality of the silicon nitride layer 106 is improved, the breakdown voltage of the memory device can be more consistent.

[0020] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.